CLAIMS

What is claimed is:

1. A substrate for testing semiconductor devices, comprising:
a semiconductor substrate having a dielectric layer on an exposed surface thereof;
at least one conductive trace on said dielectric layer;
a passivation layer over said at least one conductive trace and said dielectric layer; and
a metal-lined via in said passivation layer in electrical communication with said at least one conductive trace.

2. The substrate of claim 1, wherein said metal-lined via is formed of a size and shape to receive approximately 10% to 50% of an overall height of a substantially spherical interconnection element.

3. The substrate of claim 2, wherein said metal-lined via is formed of a size and shape to receive approximately 30% of an overall height of a substantially spherical interconnection element.

4. The substrate of claim 1, wherein said via includes sloped sidewalls.

5. The substrate of claim 1, wherein said via includes stepped sidewalls.

6. The substrate of claim 1, wherein said at least one conductive trace comprises copper.

7. The substrate of claim 1, wherein said passivation layer comprises polyimide.

8. The substrate of claim 1, wherein said metal-lined via comprises a metal from the group comprising gold, platinum, palladium, and tungsten.